



***ANALYSIS OF FLEXIBLE DESIGN OPTIONS
FOR MIXED-SIGNAL INTEGRATED CIRCUIT
PRODUCTS***

IDS.332 Final Project (draft)
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Definitions

ADC	Analog to Digital Converter
COGS	Cost of Goods Sold
DAC	Digital to Analog Converter
DSP	Digital Signal Processing
GM	Gross Margin
Hetero	Heterogeneous (integration type)
IC	Integrated Circuit
Mono	Monolithic (integration type)
NPV	Net Present Value
Rx	Receive
SiP	System in Package (integration type)
Tx	Transmit

Executive Summary

The economy of scale benefits associated with Monolithic (Mono) integration in mixed-signal Integrated Circuit (IC) product development compels companies to build big and commit early. This approach works extremely well when demand is known and customer acceptability is guaranteed. However, in the face of uncertain market demand and increasing global competition, Monolithic integration becomes less attractive due to the lack of flexibility to meet changing requirements.

In general, demand for mixed-signal IC products comes from three application spaces:

- 1) Transmit (Tx) only signal chain applications
- 2) Receive (Rx) only signal chain applications
- 3) Transceiver (Tx and Rx) signal chain applications

The purpose of this project was to investigate whether the flexible design options available from System in Package (SiP) integration improve the expected return on investment for mixed-signal IC designs (for the application spaces above) by enabling new and different integrated products that meet uncertain future demand of customers.

The following five analysis steps were used to compare options and strategies:

- 1) Step 1: Create a standard NPV valuation model to
- 2) Step 2: Perform a sensitivity analysis of the model using Monte Carlo analysis
- 3) Step 3: Calculate the NPV of a base case using static inputs
- 4) Step 4: Calculate the NPV of a base case using dynamic inputs using Monte Carlo analysis

5) Step 5: Calculate the NPV of flexible cases using dynamic inputs using Monte Carlo analysis

Based on the analysis described in this report, a well-planned System in Package (SiP) integration strategy provided the highest NPV and scored the best overall according to the evaluation metrics used in the report. The SiP Integration option pushes out the decision about when and what to integrate. This deferred commitment enables future expansion and allows different combinations of subsystems as market demand changes.

Background

The technological innovations from the semiconductor industry directly affect every aspect of our lives. From the way we communicate, travel, entertain, defend, and care for ourselves, to the way businesses build, analyze, transport, and manage resources; semiconductor technology enables it all.

Driven by increasing demand for servers/data centers, industrial automation, autonomous driving, wireless infrastructure, wearables, and the Internet of Things (IoT) [1], in 2017, the global semiconductor industry is expected to grow 12%, reaching \$378 Billion in total world-wide sales (year-over-year growth in August 2017 alone was 23% with a record breaking \$35 Billion in one month) [2][3].

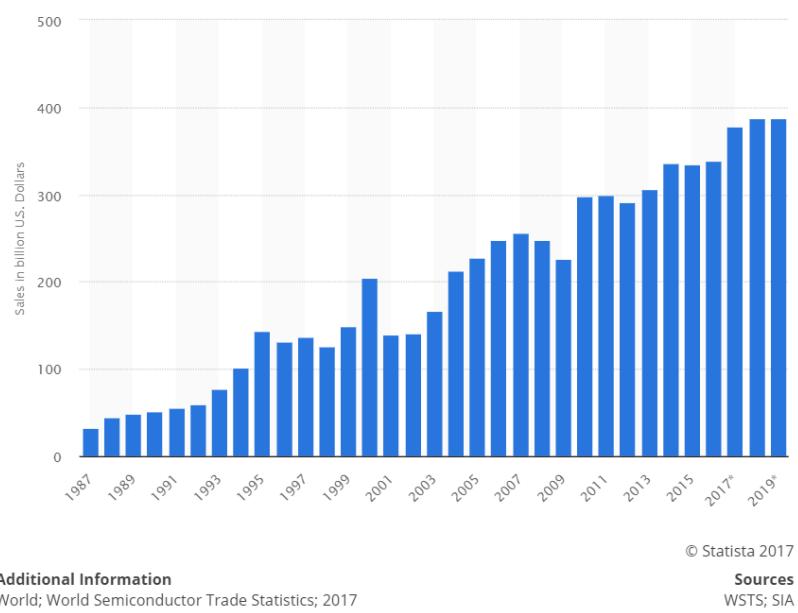


Figure 1: World-Wide Semiconductor Sales [3]

Historically, semiconductor companies pushed into smaller CMOS geometries due to the Economy of Scale (EoS) benefits associated with Moore's law [4]. However, in recent years, the benefits of making transistors smaller has been eclipsed by the need to make them more energy-efficient. At the same time, the capital investment required in these fine-line processes has increased exponentially - causing many companies to re-think their plans.

The semiconductor manufacturing process for creating CMOS IC products requires significant capital investment in expensive photo-lithographic and chemical processing [6][7]. Central to this process, circuit designers specify a set of optical masks that define the desired patterns of the different layers of the semiconductor material. This includes the definition for the individual circuits (transistors, resistors, capacitors, inductors, etc.) and the interconnecting wires. The mask sets act as a blueprint for the silicon and must follow strict design rules placed by process engineers in order to ensure manufacturability. Using specialized Computer Aided Drafting (CAD) tools to automate the design process, semiconductor fabrication plants (commonly referred to as “fabs”) go through a multiple-step sequence during which pure semiconducting material on a silicon wafer is gradually refined to create electronic circuits. The resulting wafers contain hundreds of independent ICs which are cut (“diced”) into single chips. Each chip is called a die. These die are encapsulated in special plastic, metal or ceramic packages to make IC products. Quality of the IC products is ensured by both automated and manual verification steps through this entire process. The entire process is shown graphically in Figure 2 below.

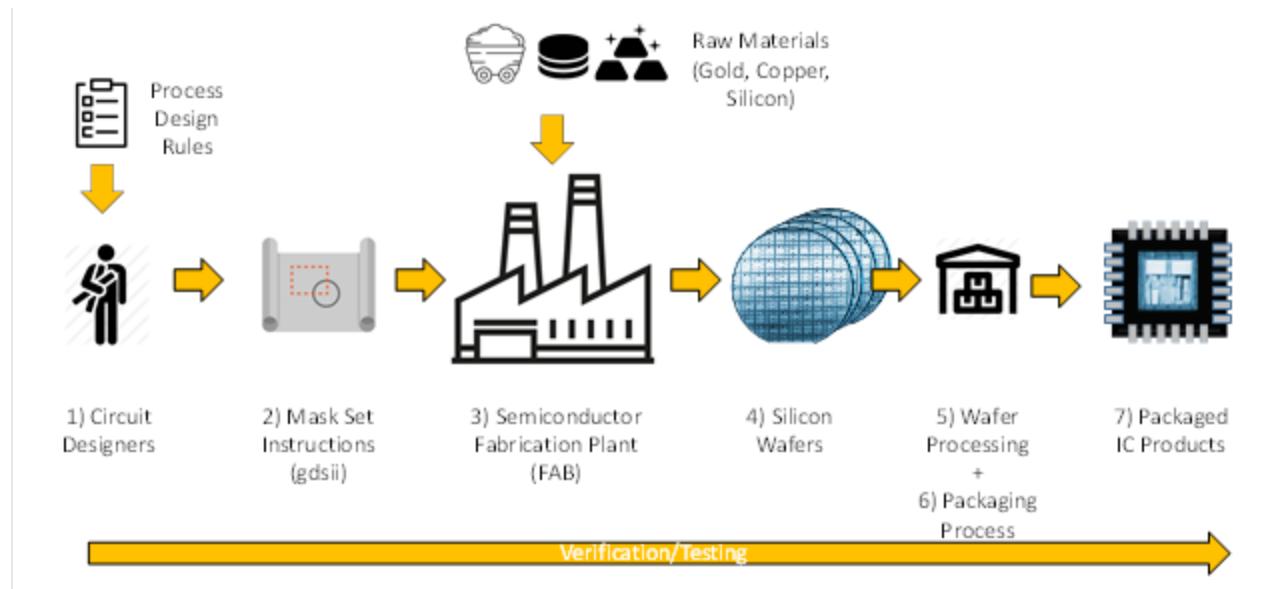


Figure 2: IC Manufacturing Process

Due to the market demand for more complex systems, higher levels of integration are required for IC products. To meet this demand, most mixed-signal semiconductor companies use at least the following integration methods to package their products [5]:

- 1) **Monolithic Integration** – A Monolithic (Mono) Integration includes a single semiconductor die contained in a single packaged device.
- 2) **Heterogeneous Integration** – A Heterogeneous (Hetero) Integration includes multiple (>1) semiconductor die connected through a semi-conductor layer (i.e. silicon interconnect) and contained in a single package without any co-packaged Resistors, Inductors or Capacitors (RLCs).
- 3) **System in Package Integration** – A System in Package (SiP) Integration includes multiple die (Mono or Hetero) that can each be manufactured on various semiconductor processes

and co-packaged with or without RLCs. The die are typically connected through a laminate or other PCB-like material. The end product is a single packaged device.

These 3 integration levels are defined in more detail below in Figure 3.

Integration Type	IC Process	IC Die	Package(s)	RLC
SiP		1 or more	2 or more	1 Few (optional)
Hetero		2 or more	1 or more	1 None
Mono		1	1	1 None

Figure 3: Defining Levels of Integration

Project Definition

Introduction

As customer demand for more functionality in smaller spaces grows, to remain competitive, companies drive toward higher levels of integration. In deep-submicron CMOS technologies (such as 28nm, 16nm and 7nm), Mono Integration has substantial Economy of Scale (EoS) benefits over Hetero and SiP Integration options. This EoS benefit compels companies to:

- 1) **Build Big** – the initial Non-Recurring Engineering (NRE) cost to create the photolithography masks are extremely expensive (millions of dollars) and cannot be re-used from one product to the next.
- 2) **Commit Early** – the mask sets are built based on simulation models of the semiconductor process and the design. Customers do not see actual working silicon until many months later. During this waiting period, companies are exposed to competitive threats.

Building Big and Committing Early increases the project risk under uncertainty and reduces the ability of the project to quickly adjust to a customer's future needs. Managing the complexity and interdependencies of a Mono Integration design becomes extremely challenging and often results in project execution unpredictability.

While often more expensive initially than Mono Integration, Hetero and SiP Integration offer the following benefits:

- 1) **Faster Turnaround Times for Interconnect Changes** – SiP (and some Hetero) Integrations can be modified much faster than Mono Integrations because the underlying laminate technology is much simpler and cheaper to modify.
- 2) **Decoupled Developments** – In Mono Integrations, one mask set is produced for each product. In Hetero and SiP Integrations, each subsystem can be given its own mask set. This allows individual subsystems to be developed independently and then assembled together in the package. It also allows different combinations of subsystems to meet changing customer demand.

- 3) **Flexibility** - By pushing out the decision about when and what to integrate, Hetero and SiP Integrations enable future expansion.
- 4) **Performance** – Since each functional block uses a separate semiconductor die, they can each be manufactured using different semiconductor processes which are optimized for RF, Analog or Digital content.

Figure 4 shows a block diagram of two different products produced from two different Mono Integration mask sets.

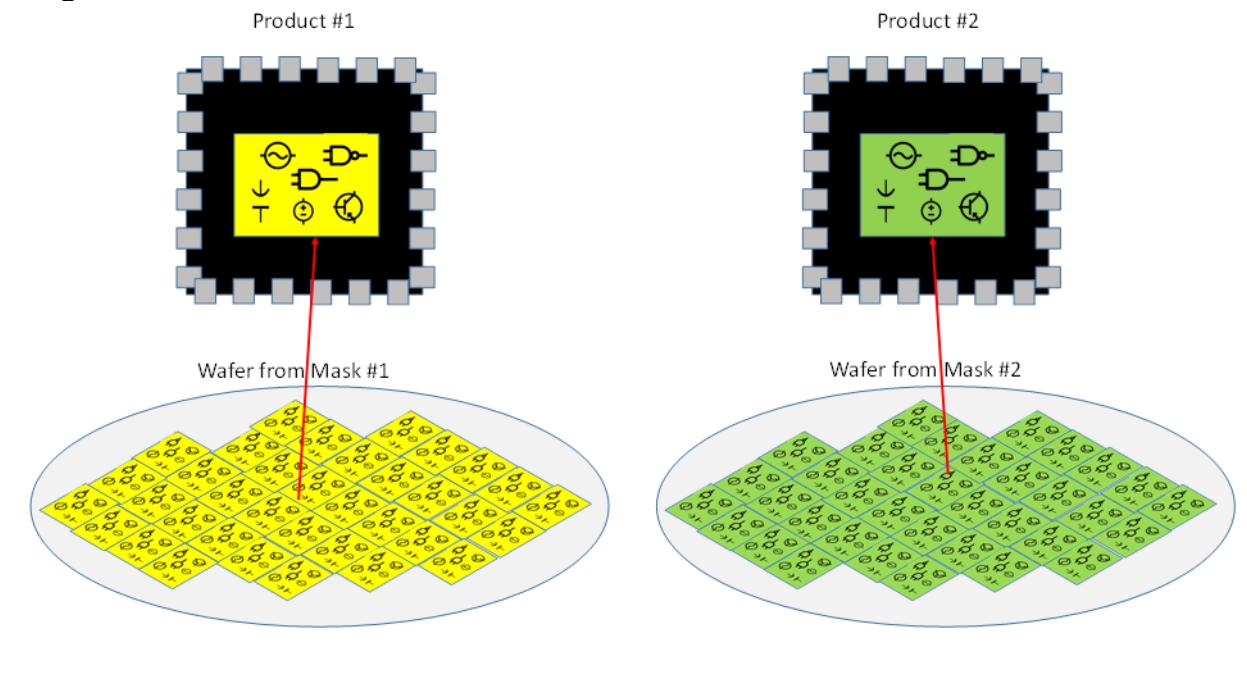


Figure 4: Monolithic Integration for two different products.

Similarly, Figure 5 shows a block diagram of two different products produced from two different SiP Integration mask sets.

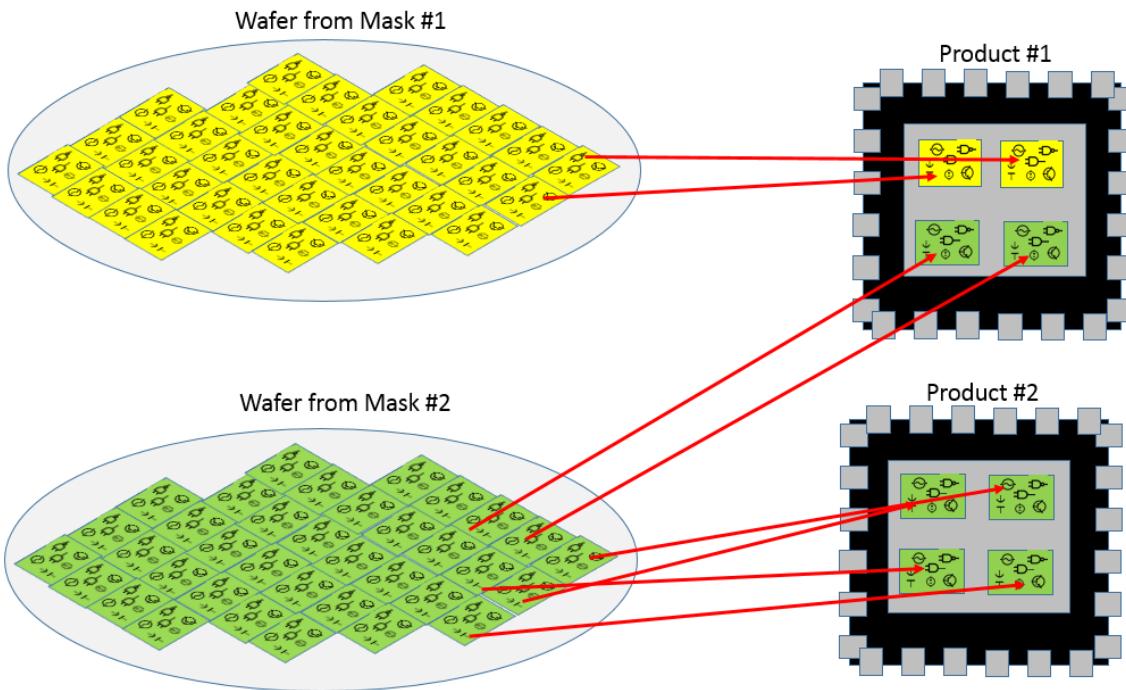


Figure 5: SiP Integration for two different products.

In both cases, the two mask sets are used to produce two products. However, the second figure provides additional flexibility.

Project Description

The purpose of this final project is to investigate whether the flexible design options available from System in Package (SiP) Integration will improve the expected return on investment for mixed-signal integrated circuit designs by enabling new and different integrated products that meet uncertain future demand of customers.

Due to time constraints on the project, I did not explore Hetero Integration options which are often more costly and only used in special circumstances where die area is a limiting factor for higher levels of integration.

System Problem Statement

To maximize the NPV of a mixed-signal Integrated Circuit (IC) product
By creating a flexible development strategy in the face of uncertainty*
Using decision rules to modify System in Package contents as demand changes

*uncertain product demand, uncertain project costs, and uncertain project execution timelines.

System Boundary

In general, demand for mixed-signal IC products comes from three application spaces:

- 4) **Transmit (Tx) Only Applications**: Customers who want the following mixed-signal Tx functionality in a single package:
 - a. 2 (or more) Analog to Digital Converters
 - b. 2 (or more) Digital Signal Processing Paths
- 1) **Receive (Rx) Only Applications**: Customers who want the following mixed-signal Rx functionality in a single package:
 - a. 2 (or more) Digital to Analog Converters
 - b. 2 (or more) Digital Signal Processing Paths
- 2) **Transceiver (Tx and Rx) Applications**: Customers who want both the Tx and Rx functionality in the same package.

For each of the applications above, a different IC product is needed. Figure 6, Figure 7, and Figure 8 below show example systems for the three mixed-signal IC products considered for this project: a transmitter, a receiver and a transceiver containing a combination of both transmit and receive signal chains.

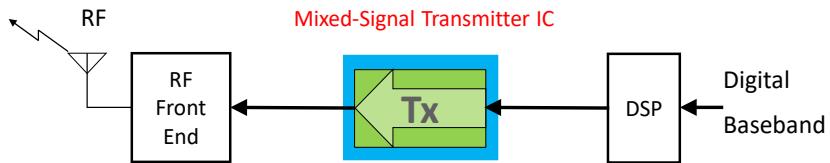


Figure 6: Mixed-Signal Transmitter IC

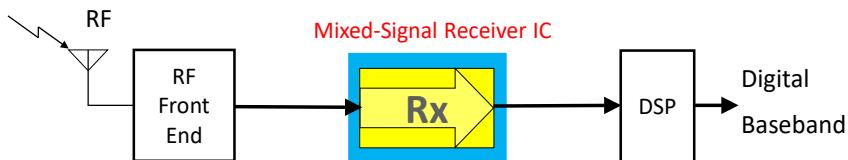


Figure 7: Mixed-Signal Receiver IC

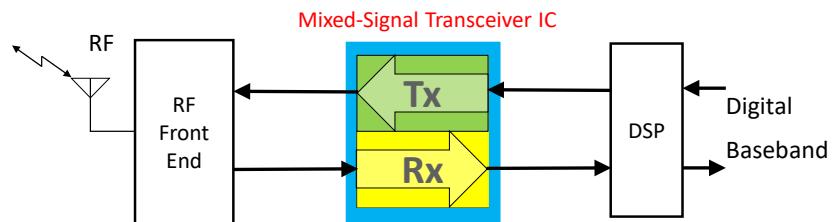


Figure 8: Mixed-Signal Transceiver IC

This project will investigate both Mono and SiP integration strategies to meet the market demands for the three applications shown above.

Analysis Steps

In order to analyze the tradeoffs associated between Mono and SiP integration; as well as exploring the value of additional flexibility options in the design process, an NPV analytical model was created to simulate different real options.

The following steps were taken to generate the analytical model used to simulate multiple options:

- 6) Step 1: Create a standard NPV valuation model
- 7) Step 2: Perform a sensitivity analysis of the model
- 8) Step 3: Calculate the NPV of a base case using static inputs
- 9) Step 4: Calculate the NPV of a base case using dynamic inputs
- 10) Step 5: Calculate the NPV of flexible cases using dynamic inputs

Each step is described in more detail below.

Step 1: Model Creation

Goal: Create a standard NPV valuation model

The standard NPV valuation model included the following:

- 1) Project Cost model: The cost model simulates both a Mono and SiP Integration for each of the following subsystems to meet the requirements described in the System Boundary section above:
 - a. A Mixed-Signal Transmit (Tx) Front End subsystem
 - b. A Mixed-Signal Receive (Rx) Front End subsystem
- 2) Project Schedule Model: Created a simple project schedule model for each of the above subsystems. The uncertainties associated with this part of the model are described in more detail in the Demand Uncertainty section below.
- 3) Demand model: The demand model simulates the expected demand for the Transmit Only, Receive Only, and Transceiver target applications described in the System Boundary section above. The uncertainties associated with this part of the model are described in more detail in the Demand Uncertainty section below.

Project Cost Assumptions

The following cost assumptions were used in the model based on information from my current employer (the numbers are either hidden or modified for this report).

Initial Capital Investment	\$250,000	at project start
<u>Development Cost</u>		
Tx Development Cost (projected)	Company Confidential	Total (design, test, etc)
Rx Development Cost (projected)		Total (design, test, etc)
Capacity Cost	\$2	per unit
<u>Silicon Cost</u>		
Mask Cost	Company Confidential	per tapeout for all layers
Wafer Cost (projected)		per wafer
Wafer % Loss (projected)	13%	Saw, Edge, Notch, Yield
<u>Test Cost</u>		
Tx Test Cost	Company Confidential	per unit
Rx Test Cost		per unit
<u>Package Cost</u>		
Tx/Rx Package Cost	Company Confidential	per unit
Tx Only Package Cost		per unit
Rx Only Package Cost		per unit

Discount Rate and Timeframe Assumption

A discount rate of 20% and a timeframe of 5 years (broken into 20 quarters) was chosen for this investigation due to the inherent uncertainties in the estimates described above, the short useful life of IC products, and the uncertainty of technological advances that could dramatically change this evaluation.

Modeled Uncertainties

The following uncertainties were identified for the project: Demand Uncertainty, Project Execution (cost/schedule) Uncertainty, Gross Margin (sale price) Uncertainty, Wafer Cost and Wafer Loss Uncertainty and are summarized in Table 1. Each uncertainty is described in more detail in the following sections.

Table 1: Summary of project uncertainties

UNCERTAINTY ASSUMPTIONS		
1 Realized demand in qtr 1 within	50%	+/- from projection
2 Additional demand by qtr 10	50%	+/- from projection
3 Additional demand after qtr 10	50%	+/- from projection
4 Annual volatility of demand growth	50%	of growth projection
5 Development Schedule Increase (mean)	18%	normal dist from projection
Development Schedule Increase (std dev)	21%	
6 Development Cost Increase (mean)	39%	normal dist from projection

Development Cost Increase (std dev)	20%	
7 Gross Margin (mean)	0%	normal dist from projection
Gross Margin (std dev)	5%	
8 Wafer Cost	10%	+/- from projection
9 Yield Variability	2.5%	+/- from projection

Many of the uncertainties listed above were found using “reasonable” estimates based on information from my current employer (the actual numbers are either hidden or modified for this report).

Demand Uncertainty

To meet the expected demand for the Transmit Only, Receive Only, and Transceiver target applications described in the System Boundary section above, the simulation assumes the following mixed-signal IC products:

- 1) **Tx Only (IC #1)**: Customers who only want the Transmit (Tx) functionality in a single package.
- 2) **Rx Only (IC #2)**: Customers who only want the Receive (Rx) functionality in a single package.
- 3) **Tx/Rx Combo (IC #3)**: Customers want both Tx and Rx functionality in the same package.

The demand for each IC is extremely volatile and was modeled independently.

Due to market pressure for higher levels of integration, the long-term demand for “Tx Only” or “Rx Only” IC products is expected to flatten; whereas, the demand for “Tx/Rx Combo” IC products is expected to steadily increase.

Table 1 below shows the underlying demand assumptions for each of the IC products.

Table 2: Underlying Demand Assumptions

DEMAND	Demand in Q1	Additional Demand in Q10		Additional Demand after Q10	
		Projected	% Increase	Projected	% Increase
Tx Only (IC#1)	87500	15%	13125	30%	26250
Rx Only (IC#2)	100000	13%	12500	25%	25000
Tx/Rx Combo (IC#3)	50000	150%	75000	200%	100000

Figure 9 below shows the static demand curves over a 5 year period (20 quarters) without any demand uncertainty.

Figure 9: Static Demand over 5 Years

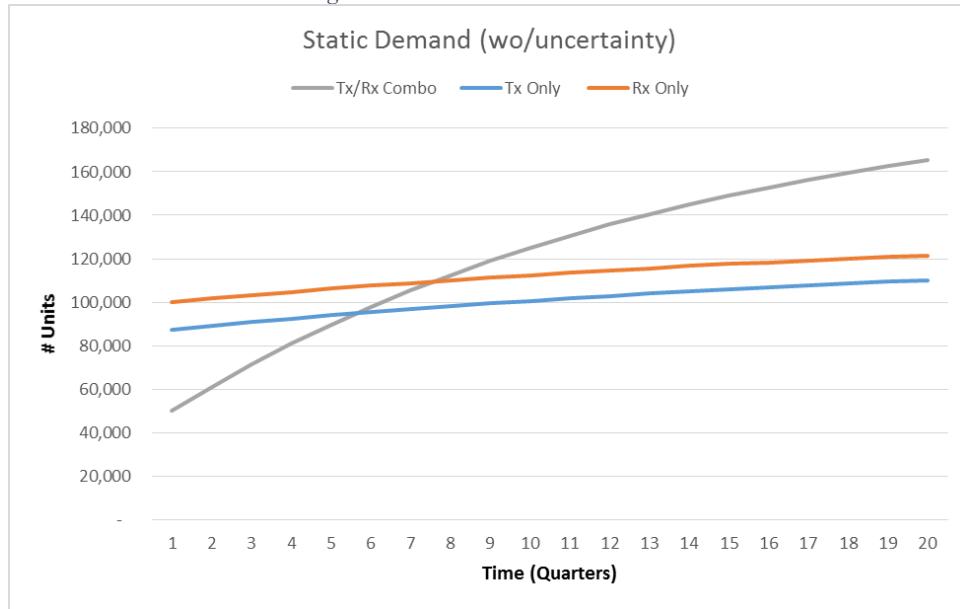


Table 2 below shows the amount of uncertainty added to the static demand model. The simulation assumes each demand uncertainty is based on a uniform probability density function.

Table 3: Demand Uncertainty (uniform)

Realized demand in Q1 within	50%	of projection
Additional demand by Q10	50%	of projection
Additional demand after Q10	50%	of projection
Annual volatility of demand growth	50%	of growth projection

Figure 10, Figure 11, Figure 12, and Figure 13 show the realized demand for four simulations under the uncertainty assumptions above over a 5 year (20 quarter) time period.

Figure 10: Realized Demand #1 (w/uncertainty)

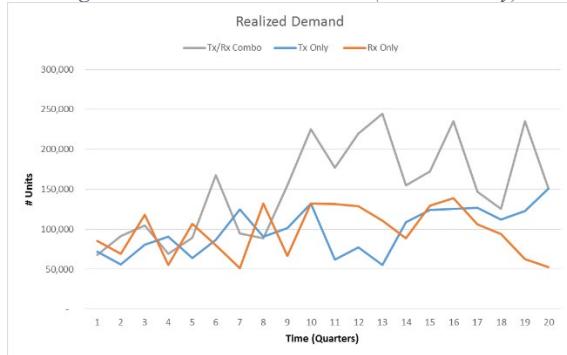


Figure 11: Realized Demand #2 (w/uncertainty)

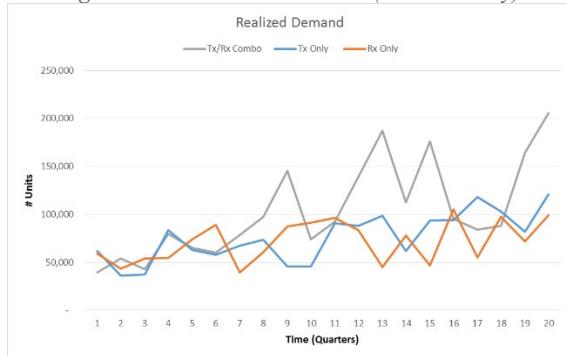
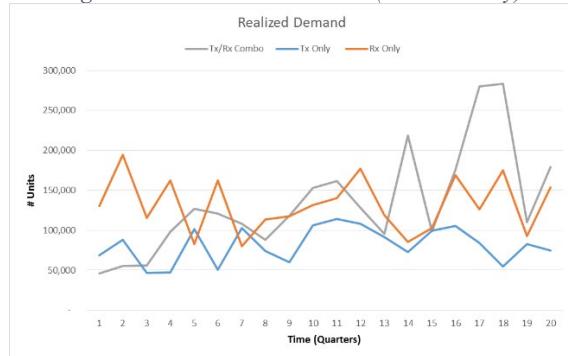


Figure 12: Realized Demand #3 (w/uncertainty)



Figure 13: Realized Demand #4 (w/uncertainty)

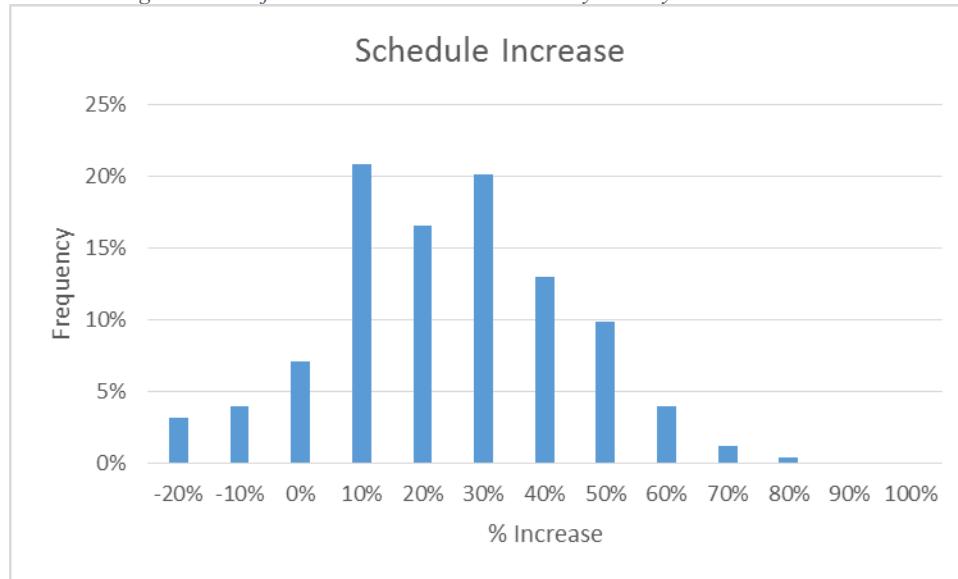


Project Development Schedule Uncertainty

Longer project development schedules impact a project's ability to capture demand for a product. By comparing the actual schedule vs the planned schedule at my current employer, I modeled the project schedule increase as a normally distributed probability density function with a mean of 18% over budget and a standard deviation of 21%.

Figure 14 below shows the resulting histogram of the normally distributed schedule increase for 254 projects. As shown below, ~15% of the projects complete on time (or early) and ~15% of the projects take 50% longer than expected.

Figure 14: Project Schedule Increase Probability Density Function

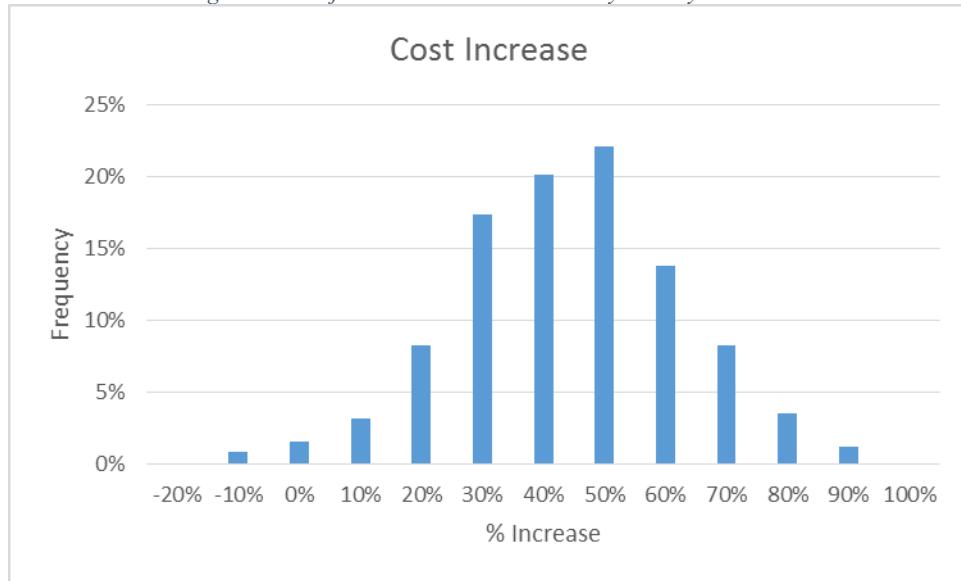


Project Development Cost Uncertainty

Similar to project schedule impact, higher development costs directly impact profitability. Often times, the project schedule can be reduced by adding additional resources. However, these resources come at a cost. By comparing the actual schedule vs the planned development cost for at my current employer, I modeled the project cost increase as a normally distributed probability density function with a mean of 39% over budget and a standard deviation of 20%.

Figure 15 below shows the resulting histogram of the normally distributed cost increase for 254 iterations. As shown below, ~15% of the projects are less than 20% over budget and ~15% of the projects are 70% over budget. Clearly, it is easier to stay on schedule than it is to stay under budget. This is likely due to the fact that additional resources can be added to pull in a schedule; whereas, it is more difficult to keep a project under-budget.

Figure 15: Project Cost Increase Probability Density Function



Gross Margin (Sales Price) Uncertainty

For this project the following equation was used to calculate the Gross Margin GM:

$$GM = 1 - \frac{COGS}{Revenue}$$

Where:

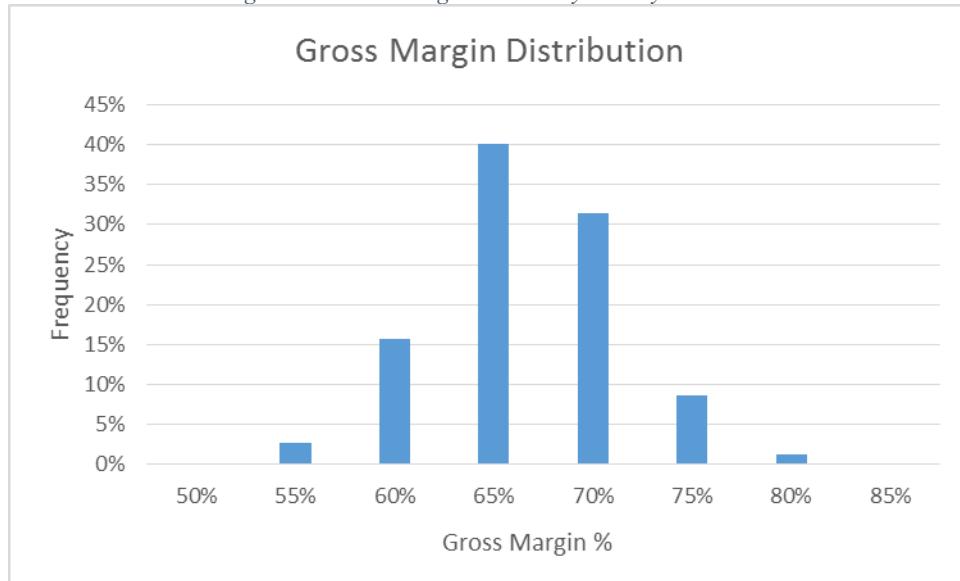
GM = Gross Margin

COGS = Cost of Goods Sold (Full - Factory Cost)

Revenue = Target Price

For companies developing mixed-signal ICs, the GM of the product is an important factor because it determines the target selling price (Price = COGS/(1-GM)). Companies in the Semiconductor industry often set GM targets around 64% [8]. However, the competitive landscape directly influences whether this is achievable. To model competitive pressure, the simulation assumes that gross margins for the product are based on a normally distributed probability density function with a mean of 64% and standard deviation of 5%. The resulting histogram of the gross margin is shown in Figure 16 for 254 iterations.

Figure 16: Gross Margin Probability Density Function



In the model, the price of the Tx/Rx products is determined solely by the GM. The price for the Tx Only and Rx Only products are based on the percentage of die area given for each function. The underlying assumptions are 1) customers will likely not pay for functionality they don't use 2) competitors could create Tx Only or Rx Only products expecting the same GM.

Wafer Cost and Wafer Loss Uncertainty

In addition to the uncertainties listed above, the wafer cost and wafer loss % (often referred to as yield) uncertainty from the manufacturing process must be taken into account. For this project, the wafer cost uncertainty was modeled as a uniform distribution +/-10% the projected cost and the wafer loss was modeled as +/-2.5% of the projected yield.

Step 2: Deterministic NPV

Goal: Calculate the NPV of a Mono Integration assuming:

- 1) static demand
- 2) static project schedule
- 3) static project costs

Figure 17 below shows a diagram of a single wafer (from a single mask set) containing a Transceiver die which is used to produce three different IC products.

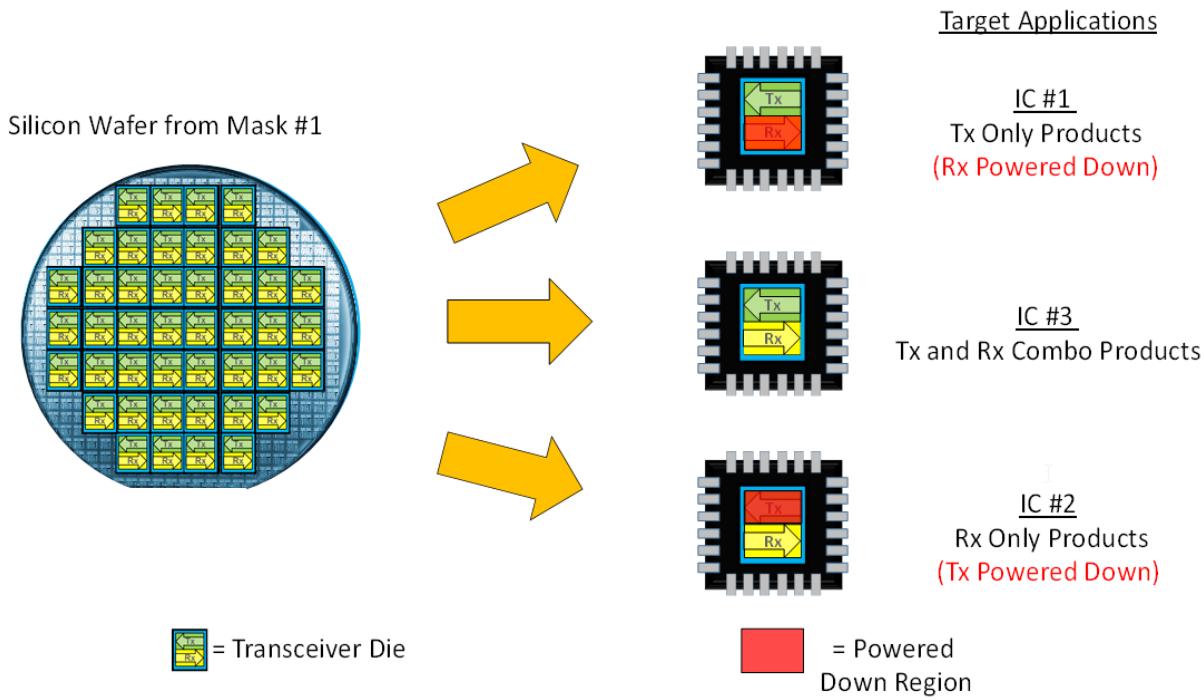


Figure 17: Monolithic Integration used to produce three ICs

As seen in the figure, each individual die in a Mono Integration contains both the Tx and Rx functionality. In a Mono Integration, it is not possible to separate them since they reside on the same piece of silicon die. For this reason, in a Tx Only application, the Rx functionality must be powered down in the device. Likewise, in an Rx Only application, the Tx functionality must be powered down in the device. Both of these scenarios result in “dark silicon” which cannot be used, but must be included as part of the full-factory cost of the product. If cost optimized competitor solutions exist, customer will likely not pay for functionality they don’t use.

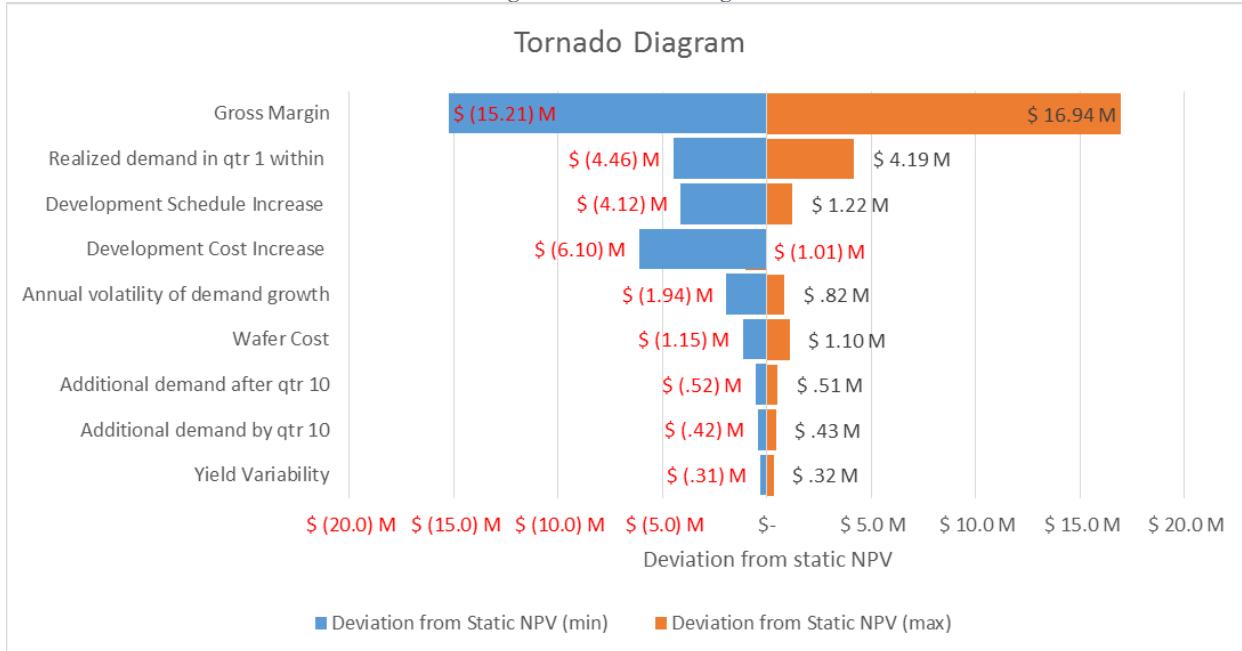
The resulting deterministic NPV for this scenario based on static inputs was **\$8.96 M**.

Step 3: Model Sensitivity Analysis

Goal: Perform a standard sensitivity analysis of the model by independently changing input variables and producing a Tornado diagram to summarize the results

The resulting Tornado diagram is shown below in Figure 18. The center point for the Tornado diagram was based on the deterministic NPV value without any uncertainty. For the base case, the deterministic NPV was ~\$9 M (as shown above).

Figure 18: Tornado Diagram



From this tornado diagram, it is clear that the Gross Margin (GM) has the highest sensitivity on the overall NPV of the project. This makes sense because the GM sets the final sales price per unit which determines the overall profitability of the device. The sensitivity to GM cannot be overstated. It is almost three times larger than the second largest uncertainty from the “Annual Volatility of demand growth”. The flexible plan in the following sections will attempt to either reduce this sensitivity or increase the center point through multiple mitigation options.

Step 4: Probabilistic NPV (Base Case)

Goal: Calculate the NPV of the Mono Integration assuming:

- 1) *uncertain demand*
- 2) *uncertain project schedule*
- 3) *uncertain project costs*

After applying the uncertainties listed above to the simulation, 2000 Monte Carlo simulations were run on the Mono Integration scenario. A histogram of the resulting simulations can be seen in Figure 19.

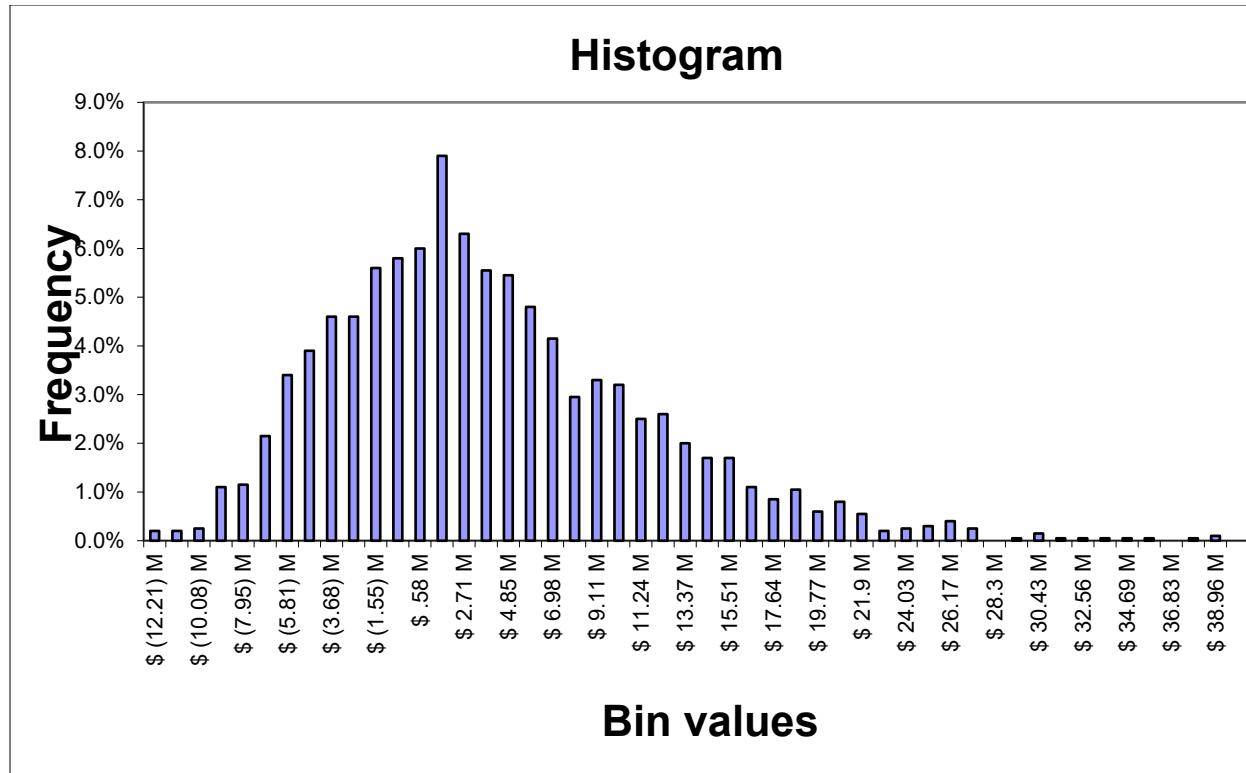


Figure 19: Histogram of 2000 Monte Carlo simulations.

The average (mean) and standard deviation of the 2000 simulation results can be seen in the table below.

Average	\$4.03
Standard deviation	\$7.85
95% Confidence Between	(\$11.35)
90% Confidence Between	(\$8.88)
80% Confidence Between	(\$6.03)
	and
	\$19.42
	and
	\$16.95
	and
	\$14.10

The 95%, 90% and 80% confidence levels above were calculated based on the following assumptions made from basic statistics

- 1) Probability follows a normal distribution function.
- 2) With 95% confidence, the target NPV will be between (mean - 1.96*std dev) and (mean + 1.96*std dev). The resulting two numbers represent the 2.5% Value at Risk (VAR_{2.5}) and 97.5% Value at Gain (VAG_{97.5}).
- 3) With 90% confidence, the target NPV will be between (mean - 1.645*std dev) and (mean + 1.645*std dev). The resulting two numbers represent the 5% Value at Risk (VAR₅) and 95% Value at Gain (VAG₉₅).
- 4) With 80% confidence, the target NPV will be between (mean - 1.282*std dev) and (mean + 1.282*std dev). The resulting two numbers represent the 10% Value at Risk (VAR₁₀) and 90% Value at Gain (VAG₉₀).

This same information in the calculations above can be gleaned by looking at the cumulative distribution function (CDF) of the actual simulation data. This data is plotted in Figure 20.

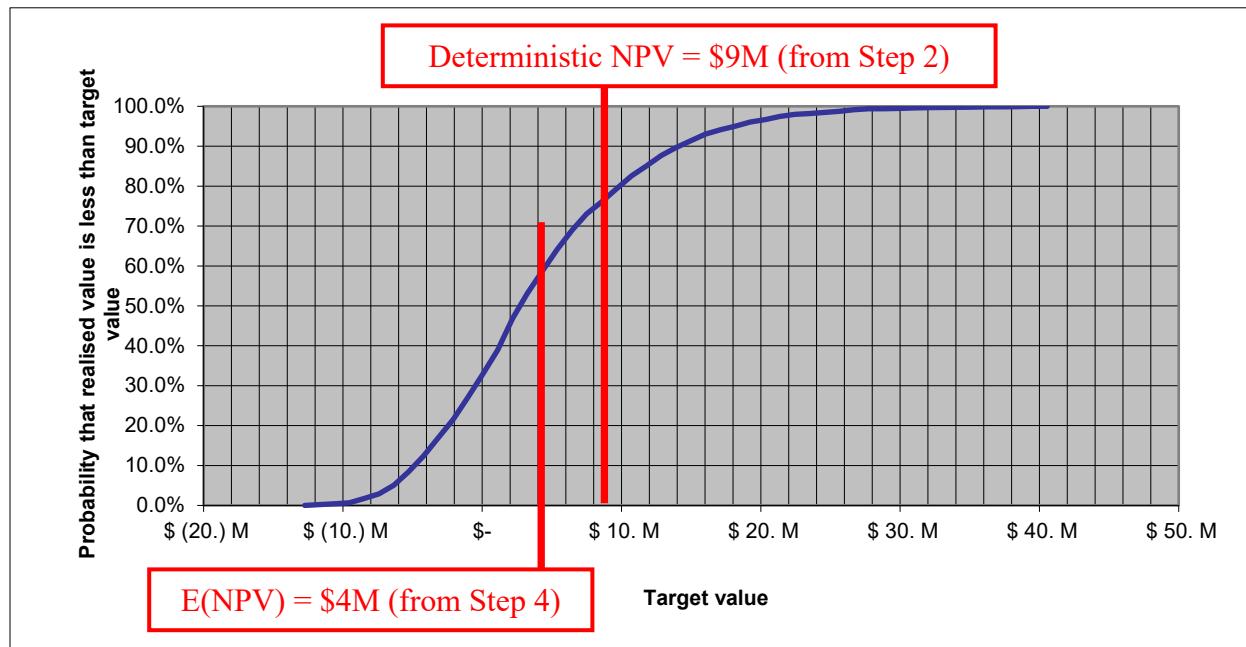


Figure 20: Cumulative Distribution Function of the Simulations

For example, by looking at the CDF, there is a 60% chance that the target value will be between -\$2M (20% of cumulative) and \$10M (80% of cumulative).

In comparison to the deterministic NPV presented earlier in Step 2 with no uncertainty, the range of results is quite significant (with 80% confidence, the outputs can vary by about +/- 248%).

Looking at the CDF data, about 78% of the simulations contained the same or lower NPV as the deterministic simulation (\$9M) found in Step 2. This is significant and clearly shows that the simplistic deterministic case does not provide enough information about the range of possible outputs. The majority of the simulations have a lower NPV and the expected average NPV of \$4M when uncertainty is added is less than half the deterministic case.

For comparison purposes, the results from this probabilistic scenario (Step 4) will be labeled as the “Base Case”.

Step 5: Flexible NPV

Calculate the NPV of both the Mono and SiP Integration with flexible design options assuming:

- 1) *uncertain demand*
- 2) *uncertain project schedule*
- 3) *uncertain project development cost*

In order to deal with the uncertainty in the project, in addition to the Base Case from Step 4, three flexible options were also considered. A comparison of the distinguishing parameters for the flexible options is shown in Table 3 below.

Table 4: Flexible Options Considered

Parameter	Base Case	Flexible Option #1	Flexible Option #2	Flexible Option #3
Integration Type	Mono	Mono	SiP	SiP
Mask Sets	1	1	1	2
Capacity Assumptions	Static	Dynamic	Dynamic	Dynamic
Capacity Dependency	None	None	$Tx = Rx$	None
Schedule Dependency (Tx)	$\max(Tx, Rx)$	$\max(Tx, Rx)$	$\max(Tx, Rx)$	Tx
Schedule Dependency (Rx)	$\max(Tx, Rx)$	$\max(Tx, Rx)$	$\max(Tx, Rx)$	Rx
Cost Dependency (Tx)	$Tx + Rx$	$Tx + Rx$	Tx	Tx
Cost Dependency (Rx)	$Tx + Rx$	$Tx + Rx$	Rx	Rx

The following sections describe each parameter in more detail.

Comparison Parameters

Integration Type & Mask Sets

These metrics simply describe whether Mono or SiP Integration was used and the number of mask sets required.

Figure 21 shows a side-by-side comparison of the 3 different wafer sets used for the flexible options. It is important to note that a separate mask set is required for each wafer option.

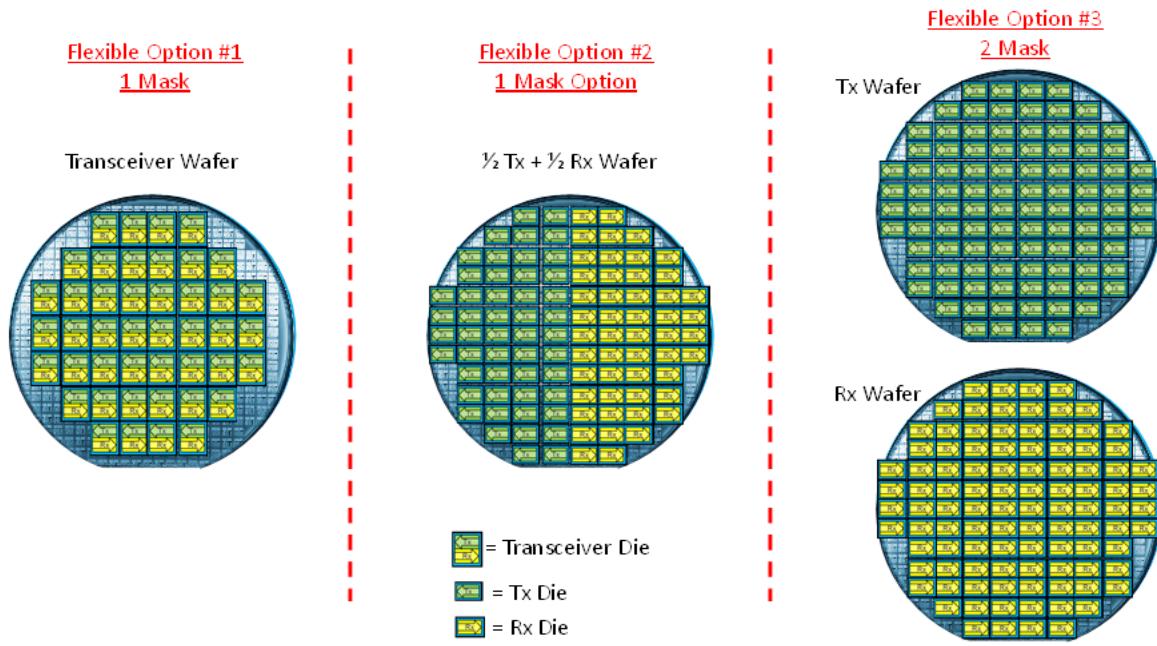


Figure 21: Mask (Wafer) Options

The product flow for the Base Case and Flexible Option #1 scenarios are shown in Figure 22. In these scenarios, one mask set is used to produce one die. This singular die is used for all three target applications and the unused functionality is powered down when not needed.

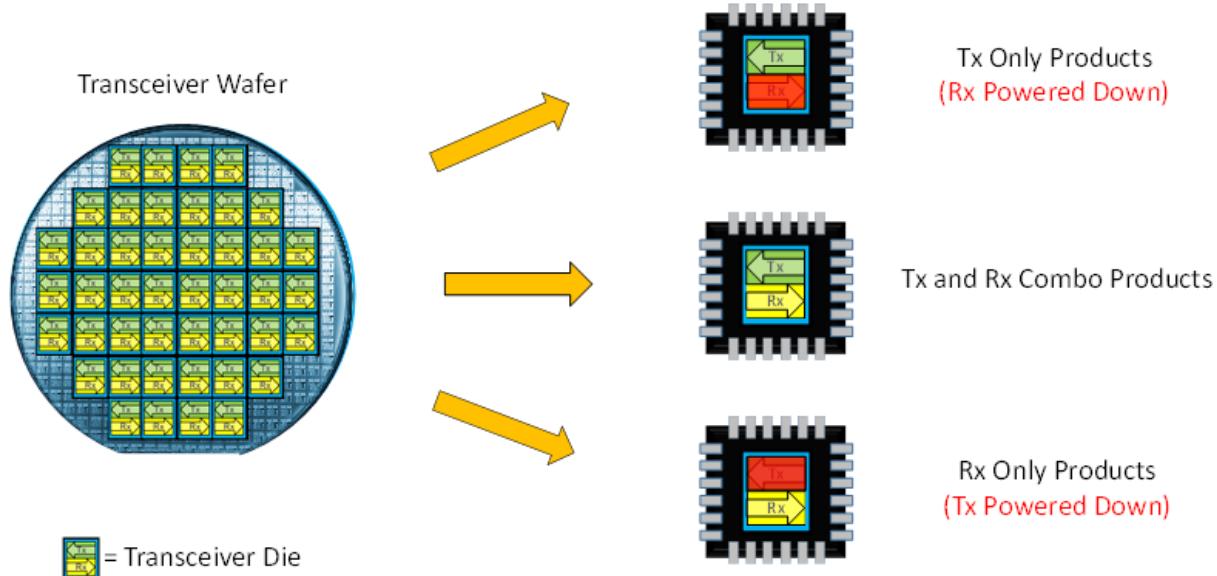


Figure 22: Base Case + Flexible Option #1

The product flow for Flexible Option #2 is shown in Figure 23. In this scenario, one mask set is used to produce two die on one wafer— one die for Rx and one die for Tx. The percentage of Tx vs Rx die is determined by the end customer, but due to wafer processing limitations, once the ratio of Tx to Rx die is set in the mask set, there is no way to change the configuration without buying a new mask set. The Tx die are used for Tx Only Products, the Rx die are used for Rx Only Products, and both die are used for Transceiver Products as shown below.

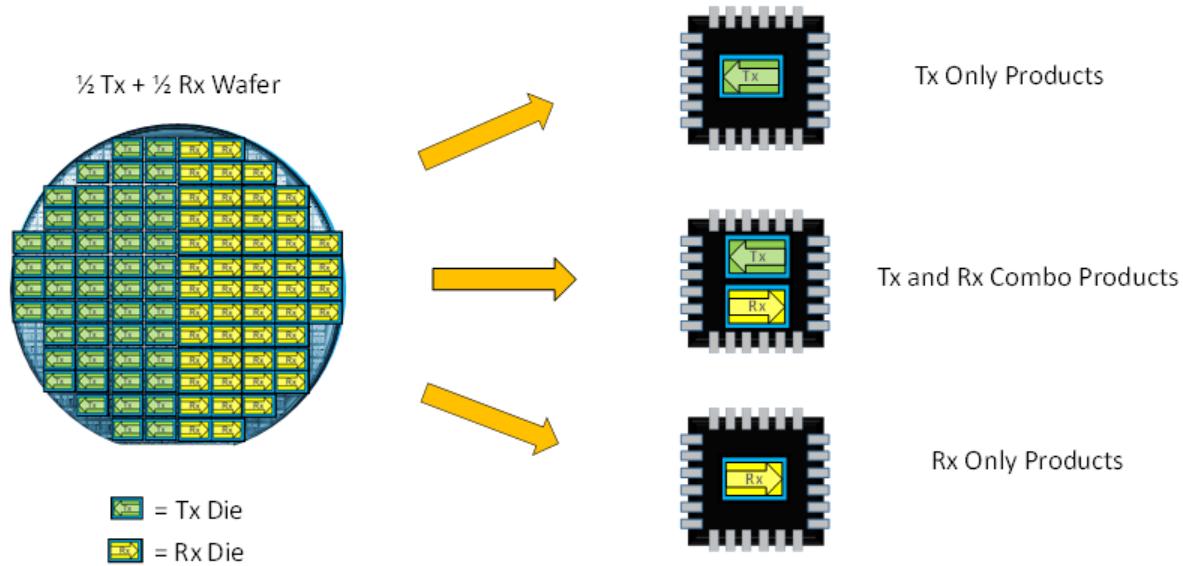


Figure 23: Flexible Option #2

The product flow for Flexible Option #3 is shown in Figure 24. In this scenario, two mask sets are used to produce two separate die – one mask set for Rx die and one mask set for Tx die. This option allows independent production control of the Tx or Rx wafers depending on demand.

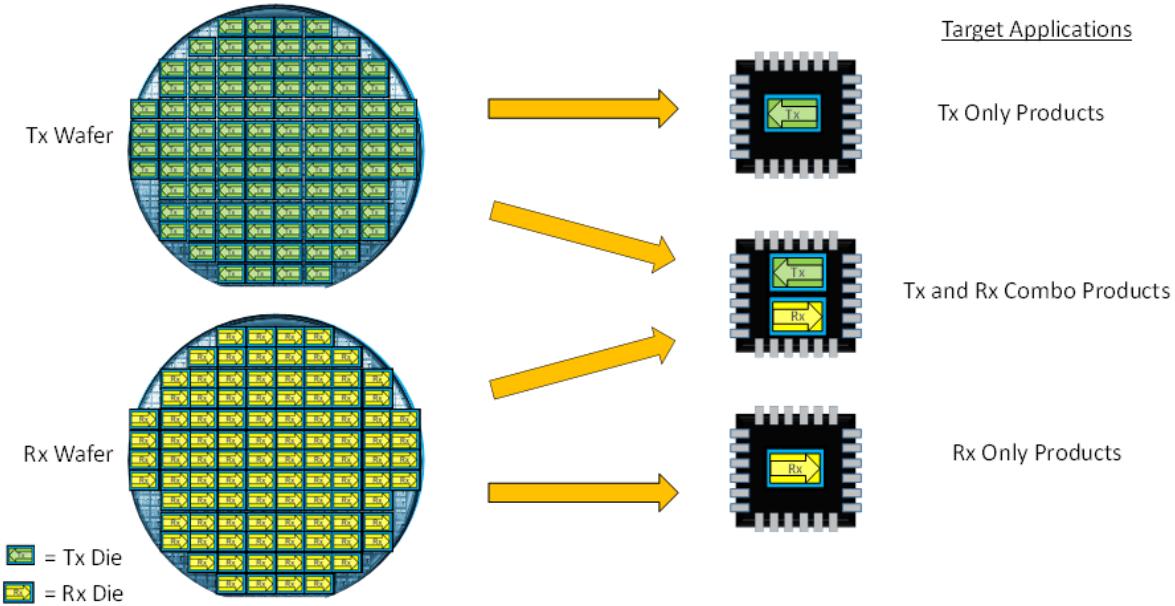


Figure 24: Flexible Option #3

Capacity

Capacity Assumptions

As in many projects, there are capacity restrictions on the project. These capacity restrictions are modelled as either static or dynamic in the simulation.

In the Base Case, the model assumes a static amount of capacity determined by the projected demand in the first quarter (Q1). If demand for a particular IC product goes beyond the capacity, revenue is lost.

In all the flexible options (#1, #2, #3), the following dynamic decision rules were applied to the model:

- 1) If the capacity/demand was $< 90\%$ for the previous two quarters, increase production capacity by 20% for the next quarter.
- 2) If the capacity/demand was $> 110\%$ for the previous two quarters, reduce production capacity by 10% for the next quarter.

The penalty for over-capacity is smaller than the penalty for lost sales due to stock outs. With this flexible option, if demand is higher than capacity, production capacity will quickly increase (by 20%). Whereas, if demand is lower than capacity, production capacity will slowly decrease (by 10%). This allows us to quickly respond to increases in demand and slowly respond to decreases.

Capacity Dependencies

As described above, due to the mask set restrictions, Flexible Option #2 requires a fixed ratio between Tx and Rx die. For this investigation, the Tx/Rx Ratio is assumed to be 50% Tx and 50% Rx.

Schedule Dependency

The Base Case, Flexible Option #1, and Flexible Option #2 utilize a single mask set for both Tx and Rx functionality. For this reason, the Tx and Rx schedules are dependent on each other.

Flexible Option #3 requires the extra capital investment of two, separate mask sets, but provides schedule flexibility. It allows the Tx Only and Rx Only developments to be decoupled from each other except as needed for the Tx/Rx Combo devices. If one development completes before the other one, it can begin generating revenue.

Cost Dependency

The Base Case and Flexible Option #1 scenarios utilized a single, Mono die containing both Tx and Rx functionality to meet all the demand (Tx Only, Rx Only, and Tx/Rx Combo). However, customers will not be willing to pay full price for the reduced functionality devices. The assumption is that customers who only want Tx or Rx functionality will only pay 50% of the Tx/Rx Combo full price. This assumption was born out of the idea that a competitor could produce a Tx Only (or Rx Only) product without the overhead of the unused Rx circuitry (or Tx circuitry).

Simulation Results

Using the spreadsheet attached to this report, two thousand Monte Carlo simulations were run on all four scenarios. Figure 25 below shows a sample NPV calculation for Flexible Option #1 and Flexible Option #3.

Year	0	0	0	0	1	1	1	1	2	2
Quarter	0	1	2	3	4	5	6	7	8	9
Realized Demand (Tx Only)	110,619	85,002	122,821	69,870	132,312	103,109	138,089	135,039	102,624	
Realized Demand (Rx Only)	115,117	157,368	121,025	174,522	145,568	139,251	103,235	124,703	163,564	
Realized Demand (Tx/Rx Combo)	40,092	53,847	95,810	92,364	61,738	147,755	68,312	133,220	111,049	
Monolithic Case										
Products Available	-									
Capacity (Tx Only)	-	-	-	-	-	-	-	-	131,250	131,250
Capacity (Rx Only)	-	-	-	-	-	-	-	-	150,000	150,000
Capacity (Tx/Rx Combo)	-	-	-	-	-	-	-	-	75,000	90,000
Total Revenue	-	-	-	-	-	-	-	-	\$7,102,546	\$7,590,712
Total COGS	-	-	-	-	-	-	-	-	\$3,292,298	\$3,472,542
Capital Expenditures (CAPEX)	\$250,000	-	-	-	-	-	-	-	-	-
Operating Expenses (OPEX)	\$1,715,365	\$1,715,365	\$1,715,365	\$1,715,365	\$1,715,365	\$1,715,365	\$1,715,365	\$5,715,365	\$712,500	\$742,500
Cashflow	(\$1,965,365)	(\$1,715,365)	(\$1,715,365)	(\$1,715,365)	(\$1,715,365)	(\$1,715,365)	(\$1,715,365)	(\$5,715,365)	\$3,097,748	\$3,375,670
DCF									\$2,096,678	\$2,175,987
Present value of cashflow	\$17,455,195									
Net present value	\$15,489,830									
SiP Case										
Products Available	-	-	-	-	-	-	-	-	131,250	131,250
Capacity (Tx Only)	-	-	-	-	-	-	-	-	131,250	131,250
Capacity (Rx Only)	-	-	-	-	-	-	-	-	150,000	150,000
Capacity (Tx/Rx Combo)	-	-	-	-	-	-	-	-	75,000	90,000
Total Revenue	-	-	-	-	-	-	-	-	\$7,102,359	\$7,590,487
Total COGS	-	-	-	-	-	-	-	-	\$2,615,656	\$2,813,038
Capital Expenditures (CAPEX)	\$250,000	-	-	-	-	-	-	-	-	-
Operating Expenses (OPEX)	\$1,715,365	\$1,715,365	\$1,715,365	\$1,715,365	\$5,715,365	\$1,977,865	\$1,977,865	\$5,977,865	\$712,500	\$742,500
Cashflow	(\$1,965,365)	(\$1,715,365)	(\$1,715,365)	(\$1,715,365)	(\$5,715,365)	(\$518,679)	(\$831,545)	(\$4,518,679)	\$3,774,203	\$4,034,949
DCF									\$2,554,529	\$2,600,964
Present value of cashflow	\$21,309,082									
Net present value	\$19,343,717									

Figure 25: NPV Sample Calculation

In this sample NPV calculation, the Tx development completed in Q4 which allowed Flexible Option #3 to capture revenue of Tx Only demand in Q5. Whereas, Flexible Option #1 could not capture this demand until Q8 after both Tx and Rx development completed in Q7.

Table 5 and Figure 25 below show the resulting expected NPV, flexibility value, and fixed cost associated with each of the flexible options when compared with the base case.

Table 5: Results from Flexible Design Options

Evaluation Metrics	Base Case	Flexible Option #1	Flexible Option #2	Flexible Option #3
NPV (mean)	\$4.03M	\$9.44M	\$14.17M	\$11.38M
NPV (std dev)	\$7.85M	\$9.63M	\$10.09M	\$9.97M
NPV (VAR ₁₀)	-\$6.03M	-\$2.91M	\$1.24M	-\$1.41M
NPV (VAG ₉₀)	\$14.10M	\$21.78M	\$27.10M	\$24.17M
Flexibility Value (mean)	-	\$5.52M	\$10.25M	\$7.46M
Fixed Cost (mean)	\$18.14M	\$18.23M	\$18.12M	\$22.34M
Fixed Cost (std dev)	\$1.41M	\$1.42M	\$1.43M	\$1.38M

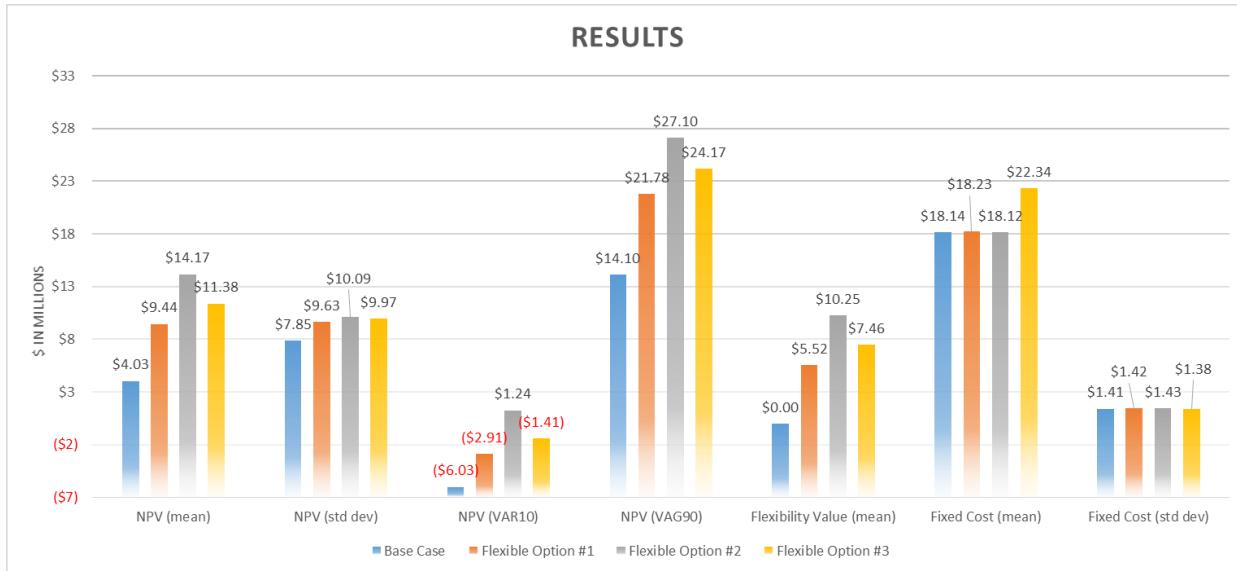


Figure 26: Results from Flexible Design Options

Finally, Figure 26 shows the both the Cumulative Distribution Functions (CDFs) and the statistical mean for each of the flexible design options.

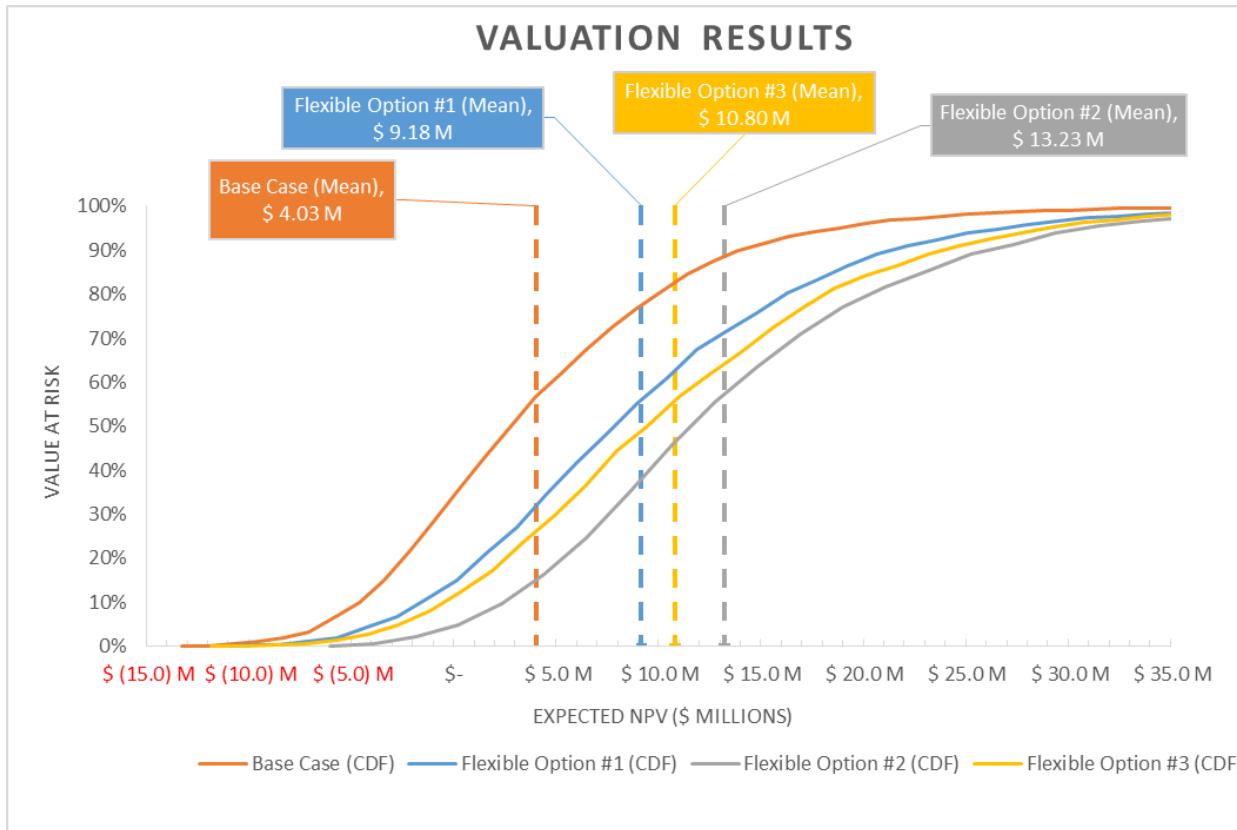


Figure 27: Value At Risk for Flexible Design Options

From these results, there is a clear benefit to both SiP Integration options (Flexible Option #2 and #3). Both of these configurations outperformed the Mono Integration options (Base Case and Flexible Option #1) in almost every category.

Decision Making

Figure 21, Figure 22, and Figure 23 below show the decision making process associated with each of the options listed above.

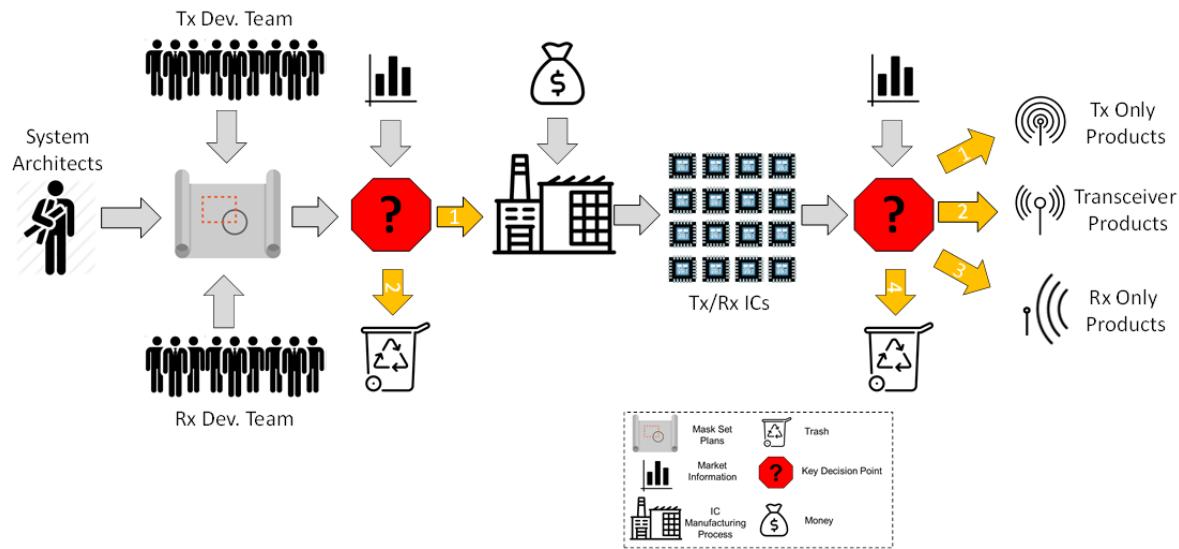


Figure 28: Decision Process for Base Case & Flexible Option #1

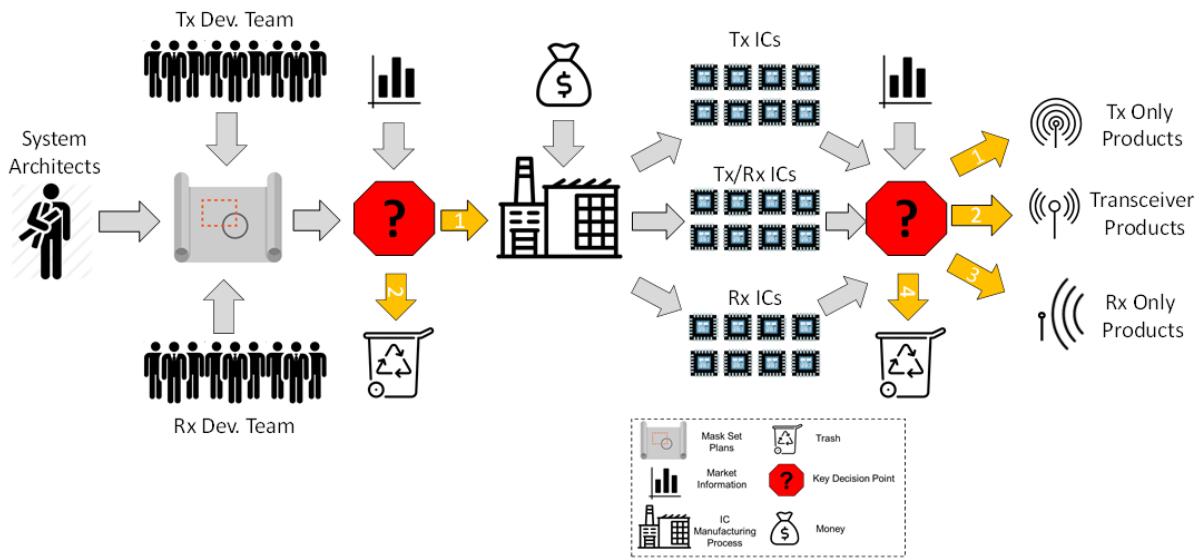


Figure 29: Decision Process for Flexible Option #2

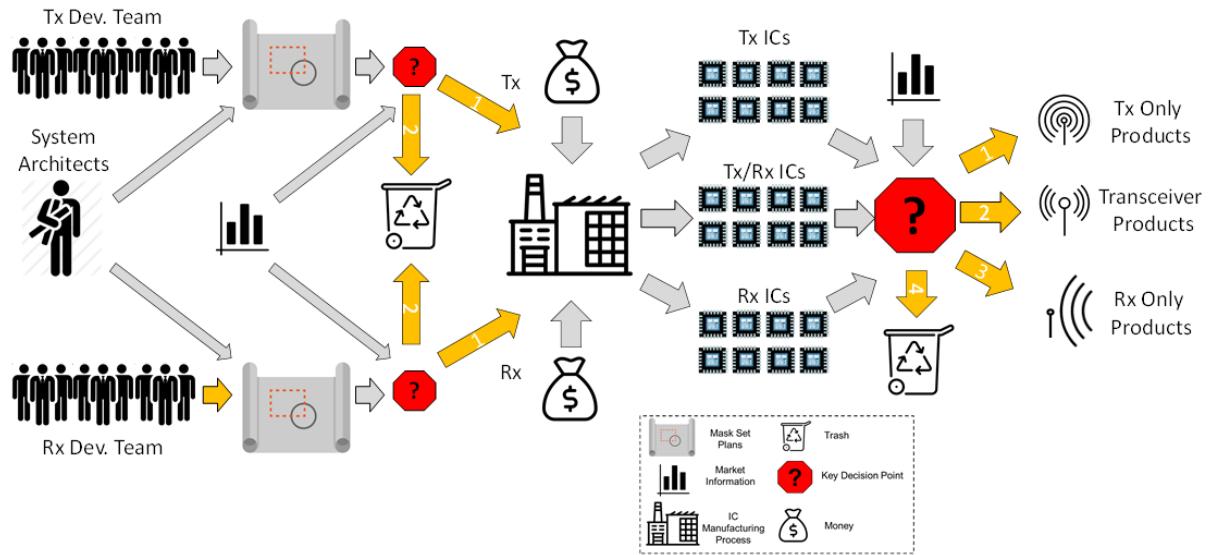


Figure 30: Decision Process for Flexible Option #3

As shown from the simulation results above, the SiP Integration options (Flexible Option #2 and #3) provide better results than the Mono Integration options. In both the SiP Integration options, the Tx and Rx functionality exist on separate die. Investing in this option at the start of the project reduces the cost of the silicon for Tx and Rx Only applications which in turn improves the Gross Margin (GM) on the Tx and Rx Only Products. By looking at the Tornado diagram in Step 2, the GM was the most sensitive input. Improvements in GM have the highest impact on the NPV. This is clearly seen in the NPV results of Flexible Option #2 and #3.

Not all flexibility created was beneficial. For example, in Flexible Option #3, the creation of two separate mask sets does not appear to be enough to offset the second mask set cost. For this reason, Flexible Option #2 provides a higher NPV and is preferred over Flexible Option #3.

Recommended Strategy

Flexible Option #2, which utilized SiP Integration, provided the highest NPV and scored the best overall according to the evaluation metrics shown above in Table 5. However, this option suffers from the same drawback as the Mono Integrations: Tx and Rx developments are coupled together and the company cannot generate revenue until both are completed. For this reason, I would recommend a hybrid approach between Flexible Option #2 and Flexible Option #3. The decision making process for this hybrid approach is shown below in Figure 31.

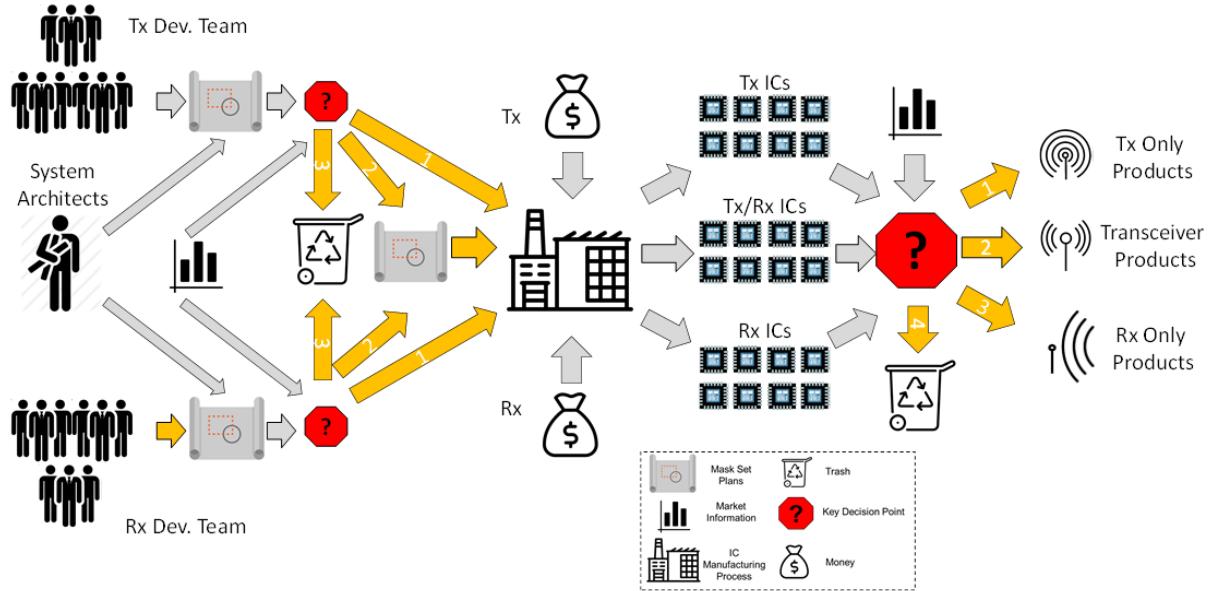


Figure 31: Decision Process for Hybrid Approach

With this new strategy, the decision regarding the number of mask sets needed (one vs two), is deferred until either the Rx or Tx developments are close to completion. If one development team is running late, management can decide to either 1) fully decouple the two developments and create an independent mask set for the completed development (may require two mask sets) or 2) wait until both developments are complete and only pay for one mask set. This decision can be made at a later point in time when additional information would be known about the market demand. This hybrid approach still takes advantage of having the Tx and Rx functionality exist on separate die which minimizes the cost of the silicon for Tx and Rx Only applications and improves the Gross Margin (GM) on those products.

In addition to the benefits above, since each functional block uses a separate semiconductor die, each could be manufactured using different semiconductor processes. This flexibility allows designers to fine-tune the performance of their functionality independent of the others.

In summary, the SiP Integration option pushes out the decision about when and what to integrate. This deferred commitment enables future expansion and allows different combinations of subsystems as market demand changes.

Final Thoughts

Going through a formal process to determine the value of flexibility has been extremely useful. It is easy to overlook the value of flexibility in the design process and having additional experience creating and running an economic valuation model with Monte Carlo inputs has provided me with new analysis tools for decision making. My results clearly show the value of additional flexible options early in the design process. I am excited to take these ideas back to my company for additional feedback and validation.

It is clear from the results of my simulation that the higher the uncertainty in a project, the higher the value of flexibility. As the global market pressure on semiconductor companies continues,

the bets are getting bigger and uncertainty exists everywhere. In the past, the economy of scale benefits associated with moving to the next semiconductor process node was considered a sure thing (Moore's Law); however, as semiconductor process advancement slows down, a flexible design approach which defers commitments becomes more valuable.

Additional Areas for Exploration

- 1) In Flexible Option #2, the ratio of Tx to Rx die per wafer could be modified prior to making the mask sets based on deferred demand for either the products.
- 2) In Flexible Option #2, if the demand for either the Tx or Rx becomes too imbalanced, an additional mask set could be created for either Tx or Rx only applications.
- 3) In order to deal with customer demand uncertainty, in the Mono Integration case, we could create new mask sets as demand increases for a particular type of product (Tx Only, Rx Only, etc).
- 4) If demand for a particular device goes below a threshold, "end of life" the product and stop production.
- 5) If the demand for the silicon never materializes, cancel the project.
- 6) If the gross margin for the project dips below 55%, cancel the project.

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